Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	246	(epitaxial or epitaxially) same (graded with (silicon or germanium))	US-PGPUB; USPAT	OR	ON	2005/01/27 17:07
L3	84	2 and dislocation	US-PGPUB; USPAT	OR	ON	2005/01/27 17:07

composition less than 20%. The etching process stops approximately at a 20% SiGe layer 14 within the compositionally graded Si.sub.1-xGe.sub.x buffer 6 and the 20% SiGe layer 14 is used as a natural etch stop.

Detail Description Paragraph - DETX (7):

[0027] The gate stack 24 is then patterned and etched into MOSFET structures. A key step is the use of a buffered oxide etchant (BOE) to undercut the gate polysilicon, forming a large "T-gate" geometry. Arsenic ion implants (35 keV, total dose 1.times.10.sup.15 cm.sup.-2) are performed to dope both the source/drain 30 and gate 24 regions at 4 perpendicular directions with a 7.degree. tilt to extend the source/drain regions under the T-gate structure. The dopant is activated via RTA at 1000.degree. C. for 1 s. Since the strained-Si layer 32 is in equilibrium, no relaxation via misfit **dislocation** introduction occurred. Blanket Ti/Al metallization is performed via e-beam deposition at a perpendicular incidence. Due to the extreme geometry of the "T-gate" FET structure and large gate LTO 26 thickness, breaks occur in the metal which isolate the source, gate, and drain regions 24 and 30 without further lithography.

Detail Description Paragraph - DETX (31):

[0045] In all of the above-mentioned SGOI or GaAs-on-insulator fabrication processes, wafer bonding is used. In order to bond two surfaces, the surfaces should be smooth enough, with a very small surface roughness. However, the as-grown SiGe layer, strained Si layer, Ge layer or GaAs layer can be rough. Typically, the compositionally graded SiGe buffer shows a very rough surface due to the cross-hatch (a **dislocation**-induced phenomenon). The CMP process is conventionally used to smooth the surface before bonding. However, as described above, CMP may induce global non-uniformity across the wafer. Moreover, in some cases, there may not be enough thickness for a surface to be polished. For example, if a layer is a strained Si etch-stop layer, its thickness is very small in order to keep it strained without relaxation, for example 10 nm.

DOCUMENT-IDENTIFIER: US 20020168864 A1

TITLE: Method for semiconductor device fabrication

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Detail Description Paragraph - DETX (2):

[0022] FIGS. 1(a)-1(d) are flow process diagrams of an experimental fabrication process of a SGOI substrate with Ge composition of 25% in accordance with one embodiment of the invention. Starting with a 4-inch Si (100) substrate 2, high quality relaxed Si.sub.0.75Ge.sub.0.25 layer 4 is grown at 900.degree. C. by UHVCVD using a compositionally graded Si.sub.1-xGe.sub.x buffer 6 technique as described in U.S. Pat. No. 5,221,413 issued to Brasen et al., which is incorporated herein by reference in its entirety. Using this technique, a compositionally graded Si.sub.1-xGe.sub.x buffer 6 can be grown epitaxially on Si substrate, which allows a relaxed SiGe layer to be grown on the top of the buffer with low threading **dislocation** density.

Detail Description Paragraph - DETX (3):

[0023] FIG. 2. is a block diagram of a compositionally graded Si.sub.1-xGe.sub.x buffer 30. The compositionally graded Si.sub.1-xGe.sub.x buffer 30 is a multi-layer structure where the Ge composition in each layer is changing gradually from a beginning value to a final value. For example, the compositionally graded Si.sub.1-xGe.sub.x buffer 30 shown in FIG. 2 has 16 layers, and the Ge composition x in the first layer is 0% and is increasing gradually to 2%, 4%, 6% until 30% in the last layer (layer 16). Such a compositionally graded Si.sub.1-xGe.sub.x buffer 30 allows a high quality relaxed Si.sub.0.7Ge.sub.0.3 layer to be grown on the top of the buffer with low threading **dislocation** density.

Detail Description Paragraph - DETX (4):

[0024] Referring to FIGS. 1(a)-1(d), a compositionally graded Si.sub.1-xGe.sub.x buffer 6 is epitaxially grown on a 4-inch Si (100) substrate 2, where the Ge composition x is increasing gradually from zero to 25% with a grading rate of 10% Ge/.mu.m. Within the compositionally graded Si.sub.1-xGe.sub.x buffer 6, a portion of the buffer 6 with Ge composition larger than about 20% forms a natural etch stop. A 2.5 .mu.m-thick undoped, relaxed Si.sub.0.75Ge.sub.0.25 cap layer 4 is then deposited, as shown in FIG. 1(a). The slow grading rate and high growth temperature result in a completely relaxed cap layer 4 with threading **dislocation** densities of .about.10.sup.5 cm.sup.-2. As shown in FIG. 1(b), the wafer 2 is then flipped over and bonded to a second Si substrate 10, which is thermally oxidized. The oxide 12 in the second substrate will become the insulator layer in the final SiGe-on-insulator substrate. The bonded pair is then annealed at 850.degree. C. for 1.5 hrs. The bonded pair is grounded to remove the donor wafer substrate 8, as shown in FIG. 1(c). The wafer 8 is then subjected to a TMAH solution to etch away a portion of the compositionally graded Si.sub.1-xGe.sub.x buffer 6 with Ge